A comparison of hashing schemes for address lookup in computer networks

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Abstract:
Using a trace of address references, the author compares the efficiency of several different hashing functions such as cyclic redundancy checking polynomials, Fletcher checksum, folding of address octets using the exclusive-OR operation, and bit extraction from the address. Guidelines are provided for determining the size of hash masks required to achieve a specified level of performance

Index Terms:
computer networks file organisation table lookup Fletcher checksum address lookup bit extraction computer networks cyclic redundancy checking polynomials exclusive-OR operation folding of address octets hash masks hashing functions hashing schemes

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A symbol based algorithm for hardware implementation of cyclic redundancy check (CRC)

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Abstract:
Describes a symbolic simulation-based algorithm to derive optimized Boolean equations for a parameterizable data width CRC generator/checker. The equations are then used to implement a data flow representation of the CRC circuit in VHDL. The VHDL description is subsequently synthesized to gates. The area and timing results of the hardware implementation are presented and compared with a conventional loop iteration technique (also described in this paper). The CRC-32 polynomial, commonly used for most computer network protocol standards, was chosen to implement the algorithm

Index Terms:
Boolean algebra cyclic codes data flow analysis equations error detection codes hardware description languages logic design logic gates polynomials redundancy timing CRC circuit CRC generator CRC-32 polynomial VHDL description area computer network protocol standards cyclic redundancy check data flow representation hardware implementation logic gates logic synthesis loop iteration technique optimized Boolean equations parameterizable data width simulation-based algorithm symbol based algorithm timing